Octal 10/100 Fast Ethernet Transceiver

Features

- Integrates eight-port 10Base-T, and 100Base-TX in a single chip
- Supports auto MDIX function and auto-negotiation
- Flexible functional configuration through either pin setting or register programming
- Supports RMII /SS-SMII interfaces
- Supports BaseLine Wander (BLW) compensation
- Provides direct drive mode and serial data latch LED display mode
- Embeds DSP-based PHY Transceiver technology to improve the cable driving performance
- Adjustable current driving capabilities
- Provides power-on LED diagnostic function
- Power supply: Selectable 3.3V/1.8V for I/O 1.8V power supply for core
- Supports Automatic Power Saving (APS) Mode
- Requires only one external clock source
- 0.18u CMOS technology
- 128Pin PQFP package
- Support Lead Free package (Please refer to the Order Information)

General description

The IP108 LF is a highly integrated octal PHY transceiver for 10Base-T, 100Base-TX Fast Ethernet applications. This device is implemented with advanced 0.18um CMOS process technology for low power consumption. For the high port count switch design such as 16 or 24 or 32-port, the IP108 LF can simplify the system design and ensure the targeted performance.

The IP108 LF can be programmed to operate in various modes through either hardware (hardware strapping pin) or software control (registers setting via SMI). It also supports RMII/SS-SMII by setting the external hardware strapping pins during power-on reset.

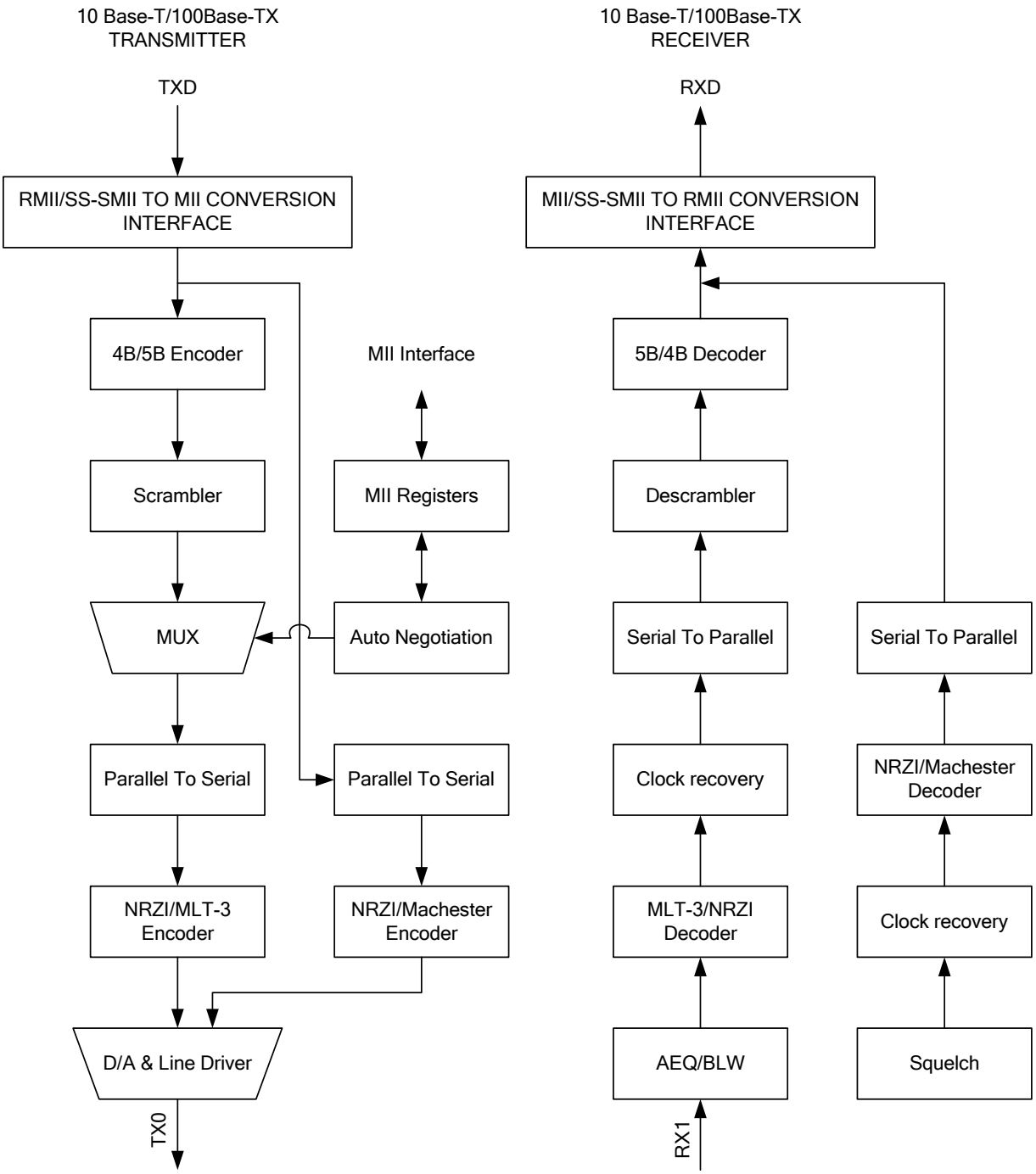
The IP108 LF contains eight independent 10/100M PHY Transceiver and includes encoder, decoder, line driver, ADC, DAC, DSP and PLL circuits for each port. The IP108 LF enters the Automatic Power Saving Mode to lower the power consumption once the link partner is disconnected. The IP108 LF just needs an external OSC or crystal as the clock source, simplifying the system design. Besides the features described above, the driving capability of IP108 LF can be trimmed to minimize the EMI effect by the advanced slew rate control technology.

Contents

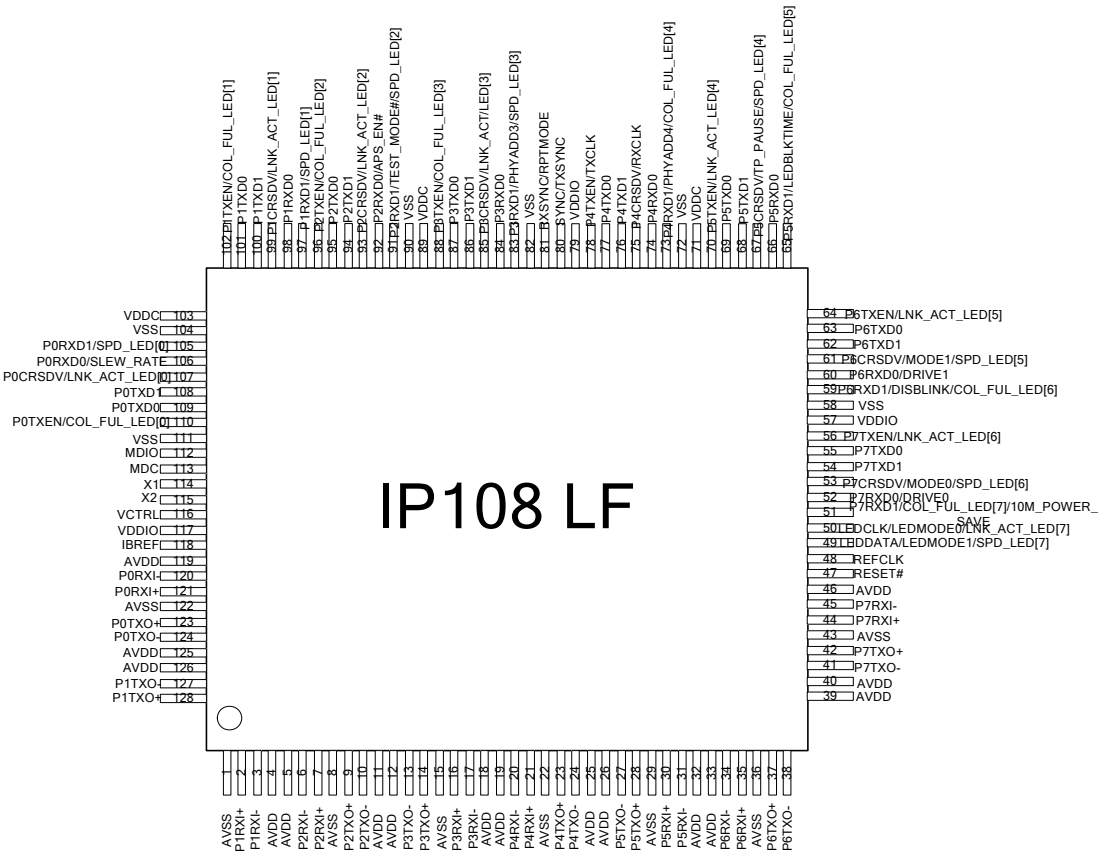
Revision History

Revision #	Change Description
IP108 LF-DS-R01	Initial release.
IP108 LF-DS-R02	Modify the pin diagram. Modify the pin description of REFCLK.
IP108 LF-DS-R03	Modify the I/O driving capability table for RMII/SS-SMII.
IP108 LF-DS-R04	Add the order information for lead free package.
IP108 LF-DS-R05	1.Modify the pin diagram, SS-SMII/RMII pins description, the default value of the latch in pins, function description, and LED mode description. 2.Modify Both RMII and SS-SMII output driving capability.
IP108 LF-DS-R06	Remove failure function.
IP108 LF-DS-R07	Revise the pin description.
IP108 LF-DS-R08	Revise the pin description.
IP108 LF-DS-R09	Revise the Register 0 description. Modify SS-SMII AC characteristics.

Block diagram



Pin Assignment



Pin Description

A: analog
D: digital
I: inputO: output
VDD: power source
VSS: power ground
C: core
IO: I/O pad

1 Pin description

Pin no.	Pin name	Type	Description
Power and Ground Pins			
71, 89, 103	VDDC	VDD, C	1.8V power for digital core
57, 79, 117,	VDDIO	VDD, IO	3.3V or 1.8V power for digital I/O.
4, 5, 11, 12, 18, 19, 25, 26, 32, 33, 39, 40, 46, 119, 125, 126	AVDD	VDD, A	1.8V power for analog circuit
58, 72, 82, 90, 104, 111	VSS	VSS, D	Digital Ground
1, 8, 15, 22, 29, 36, 43, 122	AVSS	VSS, A	Analog Ground

Pin Description (continued)

Pin no.	Pin name	Type	Description
RMII/SS-SMII Interface Pins			
55, 63, 69, 77, 87, 95, 101, 109,	P7TXD0-P0TXD0	I	TXD bit 0. These TXD bits are driven from the MAC to the PHY. These signals are synchrous to REFCLK in RMII mode and synchronous to TXCLK in SS-SMII mode. When set to RMII mode, the MAC sends the data synchronous to the REFCLK. When running at 100Mbps speed, the MAC drives the TXD at each REFCLK cycle. When running at 10Mbps speed, the MAC will keep the TXD unchanged during each ten REFCLK cycles to form a ttransmit data bit. When set to SS-SMII mode, the MAC sends 10-bit length frame, which is synchronous to TXCLK, starting with SYNC setting to high. When running at 100Mps speed, the MAC sends 10-bit TXD frame to represent one byte data. The MAC repeats the frame 10 times to form one byte data when running at 10Mbps speed.
54, 62, 68, 76, 86, 94, 100, 108	P7TXD1-P0TXD1	I	TXD bit 1. These TXD bits are driven from the MAC to the PHY and are synchronous to REFCLK in RMII mode. These pins are not used for SS-SMII and must be pulled high or pulled down.
52, 60, 66, 74, 84, 92, 98, 106	P7RXD0-P0RXD0	O	RXD bit 0. These RXD data bits are driven from the PHY to the MAC. These signals are synchronous to REFCLK in RMII mode and synchronous to RXCLK in SS-SMII mode. When set to RMII mode, the IP108 LF sends the data synchronous to the REFCLK. When running at 100Mbps speed, the IP108 LF drives the RXD at each REFCLK cycle. When set to 10Mbps speed, the MAC will keep the RXD unchanged during each ten REFCLK cycles to form a receive data bit. When set to SS-SMII mode, the IP108 LF sends 10-bit length frame, which is synchronous to the RXCLK, starting with SYNC setting to high. When operating at 100Mps speed, the IP108 LF sends 10-bit RXD frame at each RXCLK edge to represent one byte data. The IP108 LF repeats the frame 10 times to form one byte data when operating at 10Mbps speed.
51, 59, 65, 73, 83, 91, 97, 105	P7RXD1-P0RXD1	O	RXD bit 1. These RXD data bits are driven from the PHY to the MAC and synchrous to REFCLK in RMII mode. These signals are meaningless in SS-SMII mode.
56, 64, 70, 78, 88, 96, 102, 110	P7TXEN-P0TXEN	I	These signals transition synchronously at REFCLK clock edge in RMII mode. The TXEN assertion means that the valid TXD data frame is present on the TXD bus. These pins are not used for SS-SMII and should be either pulled down or pulled up by a resistor.
53, 61, 67, 75, 85, 93, 99, 107	P7CRSDV-P0CRSDV	O	These signals transition synchronously at the REFCLK edge in RMII mode. The CRSDV assertion means that RXD data frame is valid. These pins are not used for SS-SMII mode.
78	TXCLK	I	In SS-SMII mode, this pin is used as TXCLK, which is a 125MHz

			clock input to the PHY.
75	RXCLK	O	In SS-SMII mode, this pin is used as RXCLK, which is a 125MHz clock input to the MAC.
80	TXSYNC	I	This signal is used to delimit a frame of 10 bits to form one byte. The TXSYNC is used in SS-SMII mode only.
81	RXSYNC	O	This signal is used to delimit a frame of 10 bits to form one byte data, The RXSYNC is used in SS-SMII mode.

Pin description (continued)

<table>
<tr><th>Pin no.</th><th>Pin name</th><th>Type</th><th>Description</th><th>Default</th></tr>
<tr><td colspan="5">Latched Type Input Setting Pins</td></tr>
<tr><td>49, 50</td><td>LEDMODE [1:0]</td><td>IPL</td><td>These pins are used to select LED display mode upon power on reset.

<table><tr><th>LEDMODE[1:0]</th><th>Meaning</th></tr><tr><td>00</td><td>3-bit serial mode</td></tr><tr><td>01</td><td>2-bit serial mode</td></tr><tr><td>10</td><td>3-bit bi-color serial mode</td></tr><tr><td>11</td><td>Mono color direct mode</td></tr></table>
Please refer to the LED section for the detailed information.</td><td>00</td></tr>
<tr><td>51</td><td>10M_POWER_SAVE</td><td>IPH</td><td>This pin is latched upon power-on reset, and used to enable power saving mode in 10BASE mode.
1: IP108 LF support power saving mode in 10BASE mode
0: IP108 LF does not support power saving mode in 10BASE mode.</td><td>1</td></tr>
<tr><td>59</td><td>DISBNK</td><td>IPL</td><td>Disable blinking function upon power on reset
1=disable blinking
0=enable blinking</td><td>0</td></tr>
<tr><td>65</td><td>LED_BLK_TIME</td><td>IPH</td><td>This pin is used to set the blinking time of LED indicator.
1=40ms
0=120ms</td><td>1</td></tr>
<tr><td>61,53</td><td>Mode [1:0]</td><td>IPH</td><td>These pins are used to decide what operating mode is selected.
Mode[1:0] MODE
11 RMII
01 SS-SMII</td><td>11</td></tr>
<tr><td>67</td><td>TP_PAUSE</td><td>IPH</td><td>Flow control function for TP cable
1=enable flow control
0= disable flow control</td><td>1</td></tr>
<tr><td>81</td><td>RPT_MODE</td><td>IPL</td><td>This pin is latched upon power on reset and used to set the IP108LF as a repeater.This pin should be set to one by external pulled up 4.7Kohm resistor.</td><td>0</td></tr>
<tr><td>73, 83</td><td>PHY_ADDR [4:3]</td><td>IPL,IPH</td><td>These two pins will be latched to set the highest 2 bits of 5 bits PHY address upon power on reset</td><td>01</td></tr>
<tr><td>91</td><td>TEST_MODE#</td><td>IPH</td><td>This pin is latched to set the operating mode upon power on reset
1=Normal mode
0=Testing mode</td><td>1</td></tr>
<tr><td>92</td><td>APS_EN#</td><td>IPL</td><td>This pin is latched upon power on reset and used to enable the IP108 LF APS mode or not.</td><td>0</td></tr>
</table>

106	SLEW_RATE	IPH	I/O slew rate selection. 0: Slow; 1: Fast	1
99,107	Reserve pins		These pins are internal use	00

Pin description (continued)

Pin no.	Pin name	Type	Description	Default
Latched Type Input Setting Pins (continued)				
52, 60,	IO_DRIVE [1:0]	IPL	These 2 pins are latched upon power on reset and used to control I/O output driving capability Please refer to the section of I/O driving capability.	00

Pin description (continued)

Pin no.	Pin name	Type	Description
Crystal and Clock Pins			
47	RESET#	I	Reset is an active low signal and should be kept low for at least 1ms.
48	REFCLK	I/O	If x1 is active, the REFCLK will output 50Mhz clock. If x1 is inactive (pulled down), the REFCLK should be either 50Mhz or 125Mhz clock input, depending on the operating mode. 50Mhz 100ppm input for RMII This pin should be connected to GND in SS-SMII application.
114	X1	I	25Mhz crystal or OSC input pin
115	X2	O	25Mhz crystal x2
Reference Pins			
118	IBREF	A	This pin must be connected to analog ground through 6.19k resister for internal circuit use.
116	VCTRL	O	This pin is used to control the base of a PNP transistor to produce a 1.8V voltage for the power supply.
SMI Interface Pins			
112	MDIO	I/O	The MAC access to MII registers of the PHY through both MDIO pin and MDC pin. This pin should be kept at tri-state at least 700us after the reset completes. The MDIO must be pulled high by an external 1.5K resistor.
113	MDC	I	This pin should be kept at tri-state at least 700us after the reset completes. The MDC is sourced by the MAC, ranging from 0 to 25Mhz clock.
LED Control Pins			
49	LEDDATA	O	This is a serial bit stream output pin for LED display. Its data format depends on LED mode settings.
50	LEDCLK	O	This is a clock output pin for LED display. It is used to sample serial stream data.
Media dependent pins			
123,128, 9, 14, 23, 28, 37, 42,	P0TXOP-P7TXOP	A, O	These are positive transmit differential pair used for 10Base-T, 100Base-TX.
124,127, 10, 13, 24, 27, 38, 41,	P0TXON-P7TXON	A, O	These are negative transmit differential pair used for 10Base-T, 100Base-TX.
121,2, 7, 16, 21, 30, 35, 44,	PORXIP-P7RXIP	A, I	These are positive receive differential pair used for 10Base-T, 100Base-TX.
120,3, 6, 17, 20, 31, 34, 45,	P0RXIN-P7RXIN	A, I	These are negative receive differential pair used for 10Base-T, 100Base-TX.

2 Registers Description

The first six registers of the MII registers are defined by the MII specification

Register	Description
0	Control Register
1	Status Register
2	PHY Identifier 1 Register
3	PHY Identifier 2 Register
4	Auto-Negotiation Advertisement Register
5	Auto-Negotiation Link Partner Ability Register
6	Auto-Negotiation Expansion Registers

RO: Read Only
RW: Read/Write
LL: Latch Low until cleared
LH: Latch High until cleared
SC: Self Clearing

Register0: Control Register

Reg.bit	Name	Description	Mode	Default
0.[15]	Reset	1=PHY reset. This bit is self-clearing.	RW/SC	0
0.[14]	Loopback	1=Enable loopback. This will loopback TXD to RXD internally 0=Normal operation.	RW	0
0.[13]	Spd_Sel	Speed select: 1=100Mbps 0=10Mbps When the auto-negotiation is disabled, this bit can set the link speed. When the auto-negotiation is enabled, this bit is meaningless and affects no function even though it can be accessed.	RW	
0.[12]	Auto Negotiation Enable	1 = Enable auto-negotiation process. 0 = Disable auto-negotiation process. This bit can be set through SMI.(Read/Write)	RW	1
0.[11]	Power Down	1=Power down. All functions will be disabled except SMI .read/write function. 0=Normal operation.	RW	0
0.[10]	Isolate	1 = Electrically isolate the PHY from RMII/SMII/SS-SMII. PHY is still able to respond to MDC/MDIO. 0 = Normal operation	RW	0
0.[9]	Restart Auto Negotiation	1=Restart Auto-Negotiation process. 0=Normal operation.	RW/SC	0
0.[8]	Duplex Mode	Duplex mode: 1=Full duplex operation. 0=Half duplex operation. When the auto-negotiation is disabled, this bit can set the duplex mode. When the auto-negotiation is enabled, this bit is meaningless and affects no function even though it can be accessed.	RW	
0.[7:0]	Reserved			0

*SMI: Serial Management Interface, which is composed of MDC,MDIO, allows the MAC to manage the PHY.

Register1: Status Register

Reg.bit	Name	Description	Mode	Default
1.[15]	100Base_T4	0 = no 100Base-T4 capability.	RO	0
1.[14]	100Base_TX_FD	1=100Base-TX full duplex capable. 0=not 100Base-TX full duplex capable.	RO	1
1.[13]	100Base_TX_HD	1=100Base-TX half duplex capable. 0=not 100Base-TX half duplex capable.	RO	1
1.[12]	10Base_T_FD	1=10Base-TX full duplex capable. 0=not 10Base-TX full duplex capable.	RO	1
1.[11]	10Base_T_HD	1=10Base-TX half duplex capable. 0=not 10Base-TX half duplex capable.	RO	1
1.[10:7]	Reserved		RO	0
1.[6]	MF Preamble Suppression	The IP108 LF will accept management frames with preamble suppressed. IP108 LF accepts management frame without preamble. Minimum of 32 preamble bits are required for the first SMI read/write transaction after reset. One idle bit is required between any two management transactions (as defined in IEEE802.3u spec).	RO	1
1.[5]	Auto-negotiate Complete	1=Auto-negotiation process completed. Reg.4,5 are valid if this bit is set. 0=Auto-negotiation process not completed.	RO	0
1.[4]	Remote Fault	1=Remote fault condition detected. 0=No remote fault.	RO/LH	0
1.[3]	Auto-Negotiation Ability	1= auto-negotiation capable. (permanently =1) 0=Without auto-negotiation capability.	RO	1
1.[2]	Link Status	1=Link has never failed since previous read. 0=Link has failed since previous read. If link fails, this bit will be set to 0 until bit is read.	RO/LL	0
1.[1]	Jabber Detect	1=Jabber detected. 0=No Jabber detected. The jabber function is disabled in 100Base-X mode. Jabber is supported only in 10Base-T mode. Jabber occurs when a predefined excessive long packet is detected for 10Base-T. When the duration of TXEN exceeds the jabber timer (21ms),the transmit and loopback functions will be disabled and the COL LED starts blinking. After TXEN goes low for more than 500 ms, the transmitter will be re-enabled and the COL LED stops blinking.	RO/LH	0
1.[0]	Extended Capability	1=Extended register capable. 0=Not extended register capable. (permanently =1)	RO	1

Register2: PHY Identifier 1 Register

Reg.bit	Name	Description	Mode	Default
2.[15:0]	OUI	Composed of the 3rd to 18th bits of the Organizationally Unique Identifier (OUI), respectively.	RO	0243 h

Register3: PHY Identifier 2 Register

Reg.bit	Name	Description	Mode	Default
3.[15:10]	OUI	Assigned to the 19th through 24th bits of the OUI.	RO	000011b
3.[9:4]	Model Number	Manufacturer's model number 18h.	RO	011000b
3.[3:0]	Revision Number	Manufacturer's revision number 00.	RO	0000 b

Register4: Auto-Negotiation Advertisement Register

Reg.bit	Name	Description	Mode	Default
4.[15]	Next Page	0=Next Page disabled. (Permanently =0)	RO	0
4.[14]	Reserved		RO	0
4.[13]	Remote Fault	1=Advertises that IP108 LF has detected a remote fault. 0=No remote fault detected.	RW	0
4.[12:11]	Reserved		RO	0
4.[10]	Pause	1=Advertises that IP108 LF has flow control capability. 0=Without flow control capability.	RW	0
4.[9]	100Base-T4	Technology not supported. (Permanently =0)	RO	0
4.[8]	100Base-TX-FD	1=100Base-TX full duplex capable. 0=Not 100Base-TX full duplex capable.	RW	1
4.[7]	100Base-TX	1=100Base-TX half duplex capable. 0=Not 100Base-TX half duplex capable.	RW	1
4.[6]	10Base-T-FD	1=10Base-TX full duplex capable. 0=Not 10Base-TX full duplex capable.	RW	1
4.[5]	10Base-T	1=10Base-TX half duplex capable. 0=Not 10Base-TX half duplex capable.	RW	1
4.[4:0]	Selector Field	[00001]=IEEE802.3	RO	00001

Register5: Auto-Negotiation Link Partner Ability Register

Reg.bit	Name	Description	Mode	Default
5.[15]	Next Page	1=Link partner desires Next Page transfer. 0=Link partner does not desire Next Page transfer.	RO	0
5.[14]	Acknowledge	1=Link Partner acknowledges reception of FLP words. 0=Not acknowledged by Link Partner.	RO	0
5.[13]	Remote Fault	1=Remote Fault indicated by Link Partner. 0=No remote fault indicated by Link Partner.	RO	0
5.[12:11]	Reserved		RO	0
5.[10]	Pause	1=Flow control supported by Link Partner. 0=No flow control supported by Link Partner. When the auto-negotiation is enabled, this bit reflects link partner ability. (read only) When the auto-negotiation is disabled, this bit can be set by SMI. (read/write)	RW	0
5.[9]	100Base-T4	1=100Base-T4 supported by Link Partner. 0=100Base-T4 not supported by Link Partner.	RO	0
5.[8]	100Base-TX-FD	1=100Base-TX full duplex supported by Link Partner. 0=100Base-TX full duplex not supported by Link Partner.	RO	0
5.[7]	100Base-TX	1=100Base-TX half duplex supported by Link Partner. 0=100Base-TX half duplex not supported by Link Partner.	RO	0
5.[6]	10Base-T-FD	1=10Base-TX full duplex supported by Link Partner. 0=10Base-TX full duplex not supported by Link Partner. When the auto-negotiation is disabled, this bit is set when Reg.0.13=0 and Reg.0.8=1.	RO	0
5.[5]	10Base-T	1=10Base-TX half duplex supported by Link Partner. 0=10Base-TX half duplex not supported by Link Partner. When the auto-negotiation disabled, this bit is set when Reg.0.13=0,and Reg.0.8=0.	RO	0
5.[4:0]	Selector Field	[00001]=IEEE802.3	RO	00001

Register6: Auto-Negotiation Expansion Register

Reg.bit	Name	Description	Mode	Default
6.[15:5]	Reserved		RO	0
6.[4]	Parallel Detection Fault	1=A fault has been detected via the Parallel Detection function. 0=A fault has not been detected via the Parallel Detection function.	RO	0
6.[3]	Link Partner Next Page Able	1= Link Partner is Next Page able. 0= Link Partner is not Next Page able. (permanently=0)	RO	0
6.[2]	Local Next Page Able	1= IP108 LF is Next Page able. 0= IP108 LF is not Next Page able.	RO	0
6.[1]	Page Received	1= A New Page has been received. 0= A New Page has not been received.	RO/LH	0
6.[0]	Link Partner Auto-Negotiation Able	If Nway is enabled, this bit means: 1= Link Partner is Auto-Negotiation able. 0= Link Partner is not Auto-Negotiation able.	RO	0(Nway disabled)

3 Functional description

3.1 Basic Function

3.1.1 Auto negotiation

The IP108 LF provides auto negotiation function to determine the highest ability between two linked devices.
In addition, the parallel detection is also supported for making a decision on the link partner's ability which can not be determined through the auto-negotiation.

3.1.2 4B/5B encoder

The 4B/5B encoder converts the nibble data to 5-bit code group.
The 4B/5B encoder operates on 4-bit nibble and is independent of code group boundary. This encoding method is as following: All combinations of the 4-bit nibble are mapped to 5-bit code groups, plus control code groups, are implemented for a 100Mpbs operation at RMII/SS-SMII side and 125Mbps on physical medium. When the MII transmitter is enabled, the 4B data from the MII port is encoded into 5B code-groups.The transmit data is packaged by J/K codes at start of packet and by T/R codes at end of packet. When transmit error occurs during the transmitting process, the H code is sent to the medium. The idle code is sent between the gap of two packets.

3.1.3 5B/4B decoder

Performing the reverse process of the 4B/5B encoder, the 5B/4B decoder decodes the received code-groups. The 5bit data is decoded into 4 bit nibble data and then this decoded data is forwarded through to MII. The SSD is interpreted as the preamble and ESD and the idle codes are replaced by 0h.

3.1.4 Scrambler/ de-scrambler

The repetitive patterns existing in 4B/5B encoded data will result in large RF spectrum peaks. The peak in the radiated signal is reduced significantly by scrambling the transmit signal. The scrambler adds a random data generator to the data signal input, reducing the repetitive data patterns. The scrambler data is de-scrambled at receiver by adding the counterpart of the random generator at the receiver side.

3.1.5 Serial to Parallel/ Parallel to Serial

The parallel to serial block accepts the output of the scrambler, serializes the data, converts the data to NRZI and then shifts the data to the output. TXO pair carries differential NRZI data to MLT-3 transmitter.
The serial to parallel block accepts serial data from DSP receiver, and cconverts them to parallel format for further operation.

3.1.6 Jabber

The Jabber happens while TX_EN is asserted more than 60ms. When this case occurs, the IP108 LF will disable transmit function and the MII Reg.1.1 is set high until the jabber disappears. The TX_EN must be kept at low for 60ms to guarantee that this bit is cleared to zero.

3.1.7 Loop back

In this loop back mode, the IP108 LF allows the internal test opearation. By writing a 1 to bit14 of MII control register, IP108 LF will enter loop back mode. In this mode, the TXD data is internally transferred to RXD and the incoming packets on the cable are ignored.

3.1.8 Auto MDI/MDIX

In Auto MDIX mode, the IP108 LF detects the link activity for 80-100ms to determine whether it should swap both pairs. If no link activity is detected within this time, the IP108 LF waits a random time longer than 80ms and swap transmit/receive pair.

3.1.9 Auto Power Saving (APS) and Power Down mode

IP108 LF implements auto power saving function for octol ports. While detecting the cable disconnection for more than 2 sec, the IP108 LF unconditionally enters auto power saving mode. It transmits normal link pulse (NLP)-like pulse on its TXOP/TXON pins every 48ms and detects the incoming signal at RXIP/RXIN pins. The incoming signal may be 100Base-TX MLT-3 idle pattern, 10Base-T link pulses or Nway's FLP (fast link pulses). While detecting any incoming signals, the IP108 LF will be waken up from the APS mode and operate in the normal mode according to the result of the link. The APS mode is enabled upon power on reset.
Setting MII Reg.0.[11] will force the IP108 LF's corresponding port entering the power down mode, turning off all function of that port except the SMI (MDC/MDIO management interface).

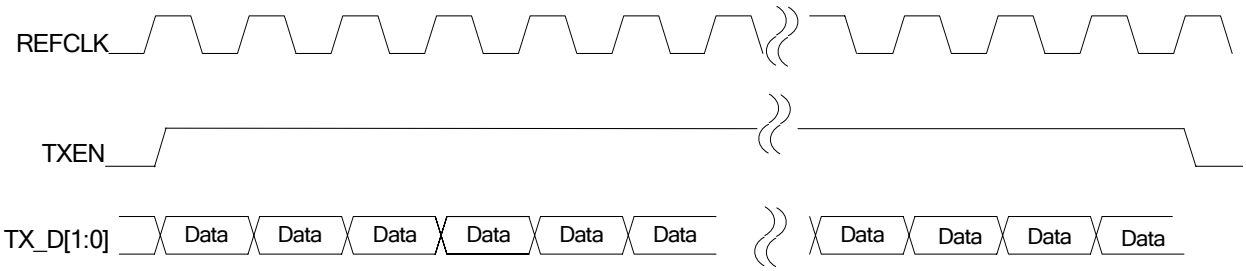
3.2 I/O Interface

3.2.1 RMII Interface

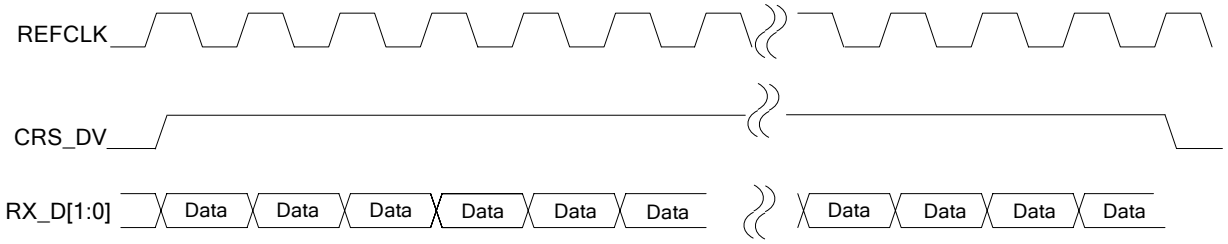
The IP108 LF is configured to RMII by setting Mode [1:0] pin upon power on reset.
For a given IP108 LF port, the RMII consists of six pins.
RXD[1:0]- di-bits(half nibble) data bus for receiver
TXD[1:0]- di-bits (half nibble) data bus for transmitter
CRS_DV- receive data control signal
TX_EN- transmit data control signal

When the RMII mode is enabled, the MAC will transfer the data through 2-bit TXD bus and assert TXEN synchronously based on 50Mhz reference clock. For 100Mbps operation, the TXD bus toggle at each rising edge of the REFCLK. In 10Mbps mode, these TXD data only change value once in every ten REFCLK cycles.

The receive data is driven from the IP108 LF to the switch MAC based on REFCLK clock rate. In order to synchronize to the local recovered clock, the IP108 LF receives data from the medium and buffer it in the internal FIFO. Since the recovered clock is not synchronous to the local REFCLK, the FIFO should cover the time difference within the whole packet time period.



Transmit RMII



Receive RMII

3.2.2 SS-SMII Interface (Source Synchronous SMII)

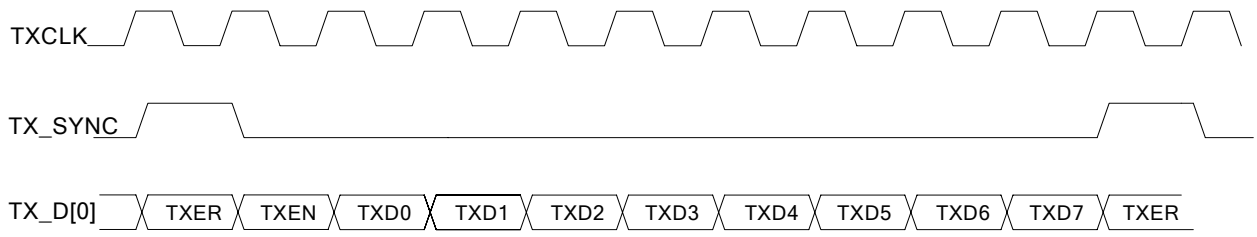
The data transfer through the SS-SMII is synchronous to both the TXCLK and the RXCLK. The TXSYNC and RXSYNC delimit the 10 bit data frame which corresponds to 8 bit data.

For the TX operation, the IP108 LF detects the TXSYNC signal at the rising edge of the TXCLK to synchronize the internal state machine. Upon detecting the high state of the TXSYNC, the IP108 LF will recognize the data present at TXD[0] as TX-ER, followed by TXEN and finally 8-port transmit data. Only the frame in which the TXEN is sampled as “high” is recognized as a valid data field.
For the RX operation, the mechanism works in a similar way. The difference is the switch controller will recognize the first data present on RXD[0] is CRS, followed by RXDV and finally 8-port receive data. The IP108 LF set the RXDV to “1” only when the valid packet is decoded.

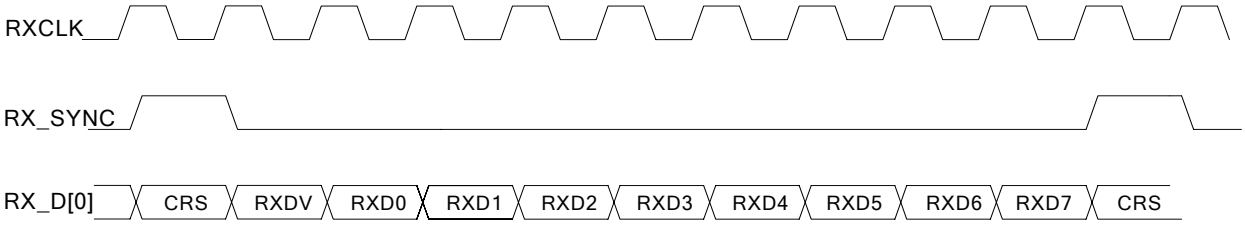
By using this clock scheme, SS-SMII timing constraints can be improved, although it will added side effect for additional traces carrying 125Mhz energy.

The IP108 LF is configured to SS-SMII by setting MODE [1:0] pins upon power on reset..
For a given IP108 LF port, the SS-SMII consists of six signals.
RXD[0]-one bit data for receiver
TXD[0]- one bit data for transmitter
TX_SYNC- This signal is driven by MAC.
RX_SYNC- This signal is driven by PHY.
TXCLK- This signal is driven by MAC
RXCLK- This signal is driven by PHY.

Note that the TXCLK, RXCLK, TX_SYNC and RX_SYNC pins are shared by all ports.



Transmit SS-SMII



Receive SS-SMII

CRS	RX_DV	RXD0	RXD1	RXD2	RXD3	RXD4	RXD5	RXD6	RXD7
X	0	RXER from previous frame	Speed 0=10Mbps 1=100bps	Duplex 0=Half 1=Full	Link 0=Down 1=up	Jabber 0=OK 1=Detected	Upper Nibble 0=Invalid 1=Valid	False Carrier 0=OK 1=Detected	1
X	1	One byte data							

During the idle state, RX_DV=0, the serial bits mean specified purpose.

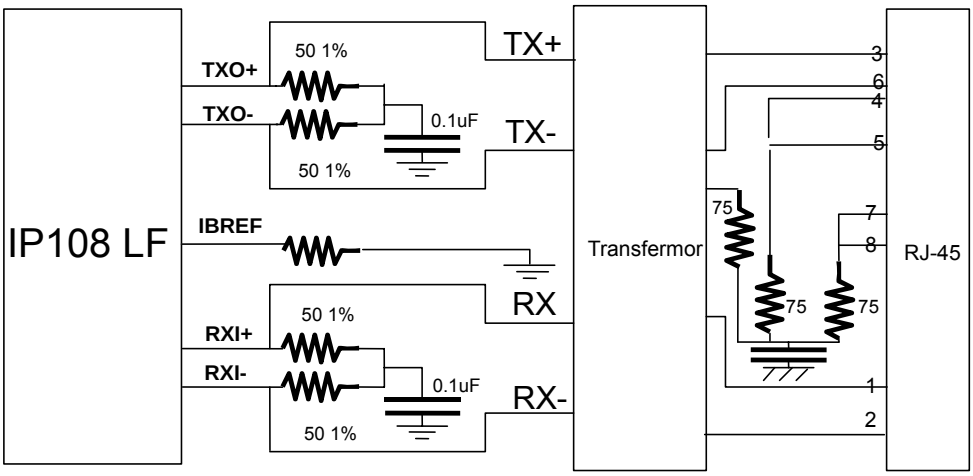
3.2.3 SMI (Serial Management interface)

SMI consists of two signals, the MDC and the MDIO. Through these two pins, the switch controller can read/configure the status of the PHY. The MDC is a clock pin, ranging from DC to 25Mhz, and the MDIO is the data transffered between the switch controller the IP108 LF.
The IP108 LF also supports preamble suppression, and it allows the Switch controller to issue read/write cycle without preamble. However, 32-bit preamble is needed for first SMI cycle after power on reset.

MII Management Interface For Read/Write Cycles								
	Preamble (32 bits)	Start bit (2 bits)	OP Code (2 bits)	PHYAD (5 bits)	REGAD (5 bits)	Turn Around (2 bits)	Data (16 bits)	Idle
Read	1……..1	01	10	AAAAA	RRRRR	Z0	D…….D	Z*
Write	1……..1	01	01	AAAAA	RRRRR	10	D…….D	Z*

MDIO must be pulled high by external 1.5Kresistor when bus is inactive. Z means high impedance

3.2.4 Guideline for the connection to a transformer



Auto MDIX Configuration

TXO+/- can be connected to the pin 1/2 of RJ-45 module, and RX+/- to 3/6, The auto MDIX function is enabled upon power on reset. The Central Tap (CT pin) must be tied high (1.8V analog Voltage) and cannot be connected to ground or unconnected.
A 75 termination resistors are needed for the unused pin of RJ45, which offers balance mechanism in order to minimize common mode noise.

3.3 Pin Setting for LED mode and driving capability

3.3.1 LED Mode Settings

IP108 LF supports either serial LED status streams or parallel direct-drive schemes for LED display. The format of LED status driving modes, as shown below, are controlled by LEDMODE[1:0] pins, which are latched upon reset. All LED statuses are represented as active-low under 3 bit and 2 bit serial modes, except Link/Act whose polarity depends on Spd status in bi-color mode or those LED pins whose polarity depends on the initial setting of pin under mono color direct mode (e.g. pin51 COL/FUL_LED[7]).

LEDMODE[1:0]		Mode	Output sequences(pins)
00		3-bit serial stream	Col / Fulldup, Link/Act, Spd
01		2-bit serial stream	Spd, Link/Act
10		3-bit for Bi-color LED	Col / Fulldup, Link/Act, Spd
11		Mono-color LED direct-drive	Col / Fulldup, Link/Act, Spd

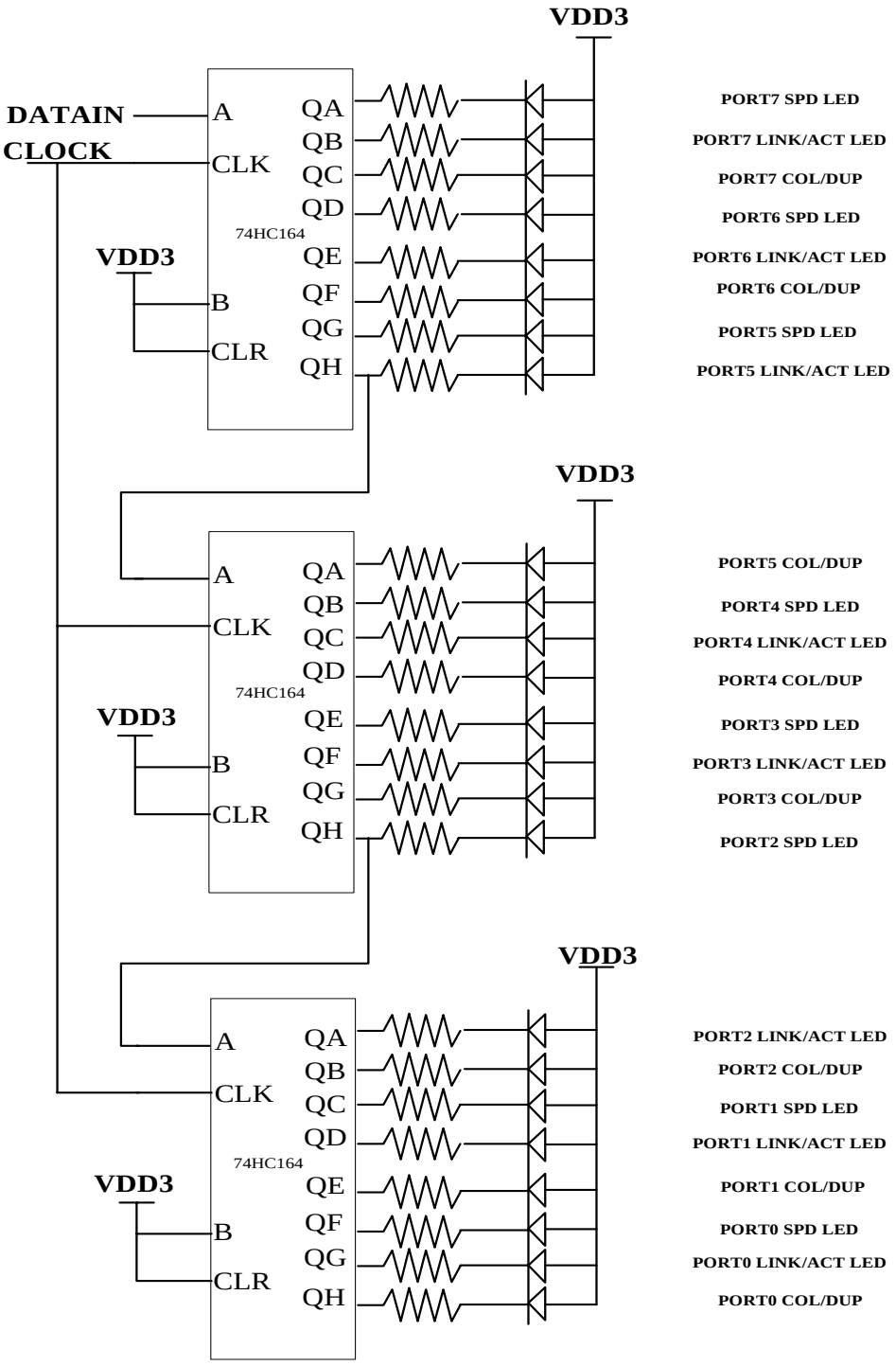
LED Indication	Description
Col / Fulldup	Col, Full duplex Indicator. Blinking every 40 or 120ms depends on LED_BLNK_TIME setting when collision happens. Low for full duplex, and high for half duplex mode.
Link / Act	Link, Activity Indicator. For 3-bit serial stream mode, low for link established. For 3-bit Bi-color LED mode and 100Mb/s, the Link/Act is high for link established. For 3-bit Bi-color LED mode and 10Mb/s, the Link/Act is low for link established. The LED blinks every 40 or 120ms when the corresponding port is transmitting or receiving.
Spd	Speed Indicator. Low for 100Mb/s, and high for 10Mb/s.

3.3.2 LED blinking setting time

The IP108 LF also provides 40/120ms LED blinking time setting through LED_BLNK_TIME pin upon power on reset, The LED's blinking time of the Col/Fulldup and the Link/Act will change according to this pin setting.
For bi-color Link/Act/Spd, the LED blinking time is not affected by LED_BLNK_TIME.

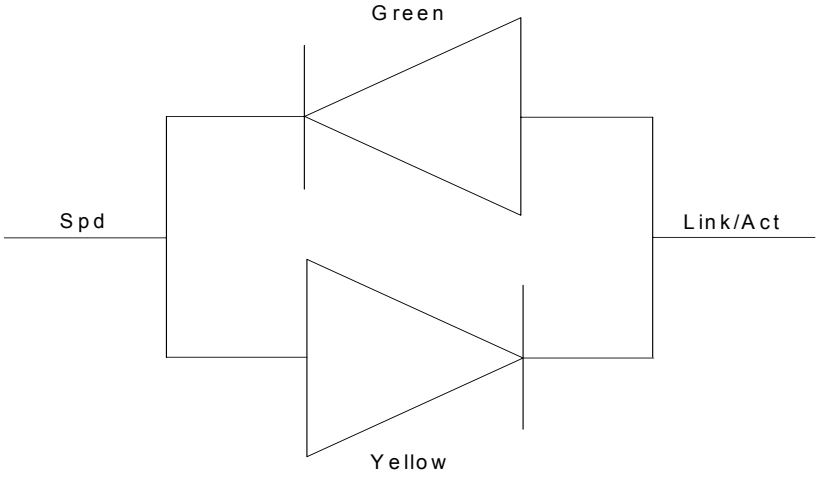
3.3.3 Serial stream sequence

Bits stream are output sequentially from port0 to port7 .For 2-bit serial stream mode, the sequence is Spd at first and then Link/Act. For 3-bit serial stream mode, the sequence is Col/Fulldup, Link/Act, then Spd.



Exteranl TTL for 3 Bit Serial Stream LED Mode

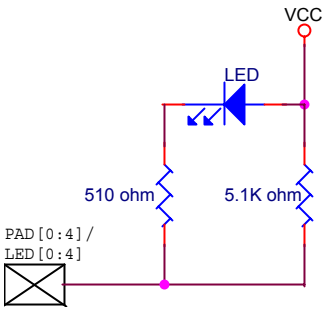
3.3.4 Bi-color Configuration



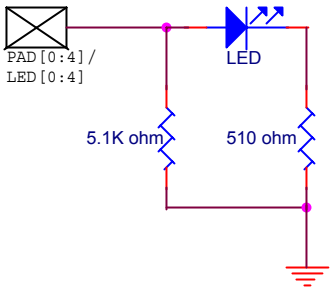
Spd	Link/Act	LED indication	Bi-color state
0	0	No link	None
0	1	100Mbps and Link	Green
1	0	10Mbps and Link	Yellow

3.3.5 LED direct drive mode configuration

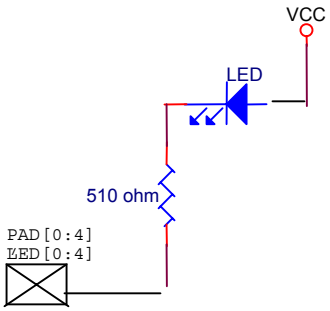
When the IP108 LF is set to LED mono color direct-drive mode, the external setting required for strapping and LED usage must be considered in order to avoid contention. Specifically, when the LED outputs are used to drive LEDs directly, the active state of each output driver is dependent on the logic level sampled by the corresponding initial setting input upon power-on reset. For example, as following figure shows, if a given initial setting input is resistively pulled high then the corresponding output will be configured as an active low driver. As the figure shown below, if a given initial setting input is resistively pulled low, the corresponding output will be configured as an active high driver. The initial setting pins should not be connected to GND or VCC directly, they must be pulled high or low through a resistor (ex 5.1KΩ). If no LED indications are needed, the components of the LED path (LED+510Ω) can be removed.



Initial Setting= logic 1
LED indication = active low



Initial Setting = logic 0
LED indication= active High



No Initial Setting
LED indication = active low

When the SS-SMII and LED mono color direct mode is used (LEDMODE[1:0]==11)			
PIN#	**PIN NAME**	**PIN#**	**PIN NAME**
49	SPD_LED [7]	83	SPD_LED [3]
50	LNK/ACT_LED [7]	85	LNK/ACT_LED [3]
51	COL/FUL_LED [7]	88	COL/FUL_LED [3
53	SPD_LED [6]	91	SPD_LED [2]
56	LNK/ACT_LED [6]	93	LNK/ACT_LED [2]
59	COL/FUL_LED [6]	96	COL/FUL_LED [2]
61	SPD_LED [5]	97	SPD_LED [1]
64	LNK/ACT_LED [5]	99	LNK/ACT_LED [1]
65	COL/FUL_LED [5]	102	COL/FUL_LED [1]
67	SPD_LED [4]	105	SPD_LED [0]
70	LNK/ACT_LED [4]	107	LNK/ACT_LED [0]
73	COL/FUL_LED [4]	110	COL/FUL_LED [0]

3.3.6 Pin setting for I/O characteristics

Driving capability control DRIVE [1:0] for RMII/SS-SMII data pins

	1.8volt		3.3volt	
50MHz(RMII)	00	2mA	00	4mA
	01	8mA	01	2mA
	10	4mA	10	8mA
	11	4mA	11	12mA
125MHz(SS-SMII)	00	12mA	00	2mA
	01	4mA	01	8mA
	10	8mA	10	12mA
	11	8mA	11	4mA

Driving capability control DRIVE [1:0] for RMII/SS-SMII clock pins

	1.8volt		3.3volt	
50MHz(RMII)	00	2mA	00	4mA
	01	8mA	01	2mA
	10	4mA	10	8mA
	11	4mA	11	12mA
125MHz(SS-SMII)	00	12mA	00	4mA
	01	8mA	01	12mA
	10	12mA	10	12mA
	11	12mA	11	8mA

Operational Description

4.1 Resetting the IP108 LF

The IP108 LF can be initialized through 3 ways, including 1: power on reset, 2:Hardware reset, 3:Software reset via setting MII register. The reset must be kept low for at least 1ms. LED will blink upon power on if DISBLINK pin is set to “low” during reset.

4.2 Transmit Function and Receive Function

100Base-TX Mode

While TX_EN is asserted, the IP108 LF converts TXD data from RMII/SS-SMII interface into 5 bit code group data starting with first two code groups called SSD (J/K code groups). The data code groups following the SSD are transmitted as long as TX_EN keeps in high state. Upon TX_EN goes low, T/R code groups will be appended to the last data code group

During inter-packet gap, idle code groups are transmitted, keeping the signal transition for the link partner to synchronize the clock. The transmit path includes 4B/5B encode, Scrambler, parallel to serial, NRZ to NRZI encoder, NZRI to MLT-3 encoder. The scrambling technology can average signal’s power energy. The wave shaping filter can reduce EMI effect.

While SSD is detected at receiver side, the TX_DV is asserted within several bit time. The receive path includes MLT-3 to NRZI decode, NRZI to NRI decode, serial to parallel, De-scrambler, and 5B/4B decode, MII to RMII /SS-SMII conversion.

On chip PLL circuit extracted clock from the incoming data stream. This recovered 125Mhz clock is used to generate the 25Mhz RX_CLK signal for MII interface. Active hybrid DC wander correction can compensate baseline wander, reducing the bit error rate.

10Base-T Mode

Unlike the MLT-3 code used in 100 base-T mode, the IP108 LF use Manchester encoder/decoder to transmit/receive data. The Manchester code provides enough transition for the link partner to recover the clock and keeps the power energy at the allowable level.

The opeartion of 10 Base-T mode follows the 802.3 standard. Both full-duplex and half duplex modes are supported by the IP108 LF.

4 Layout guideline

The following sections include recommendations for the IP108 LF board layout guidelines.
– General layout guideline
– Twisted pair guideline
– RMII layout guideline
– SS-SMII layout guideline
– Power filter recommendation
– MDC and MDIO recommendation

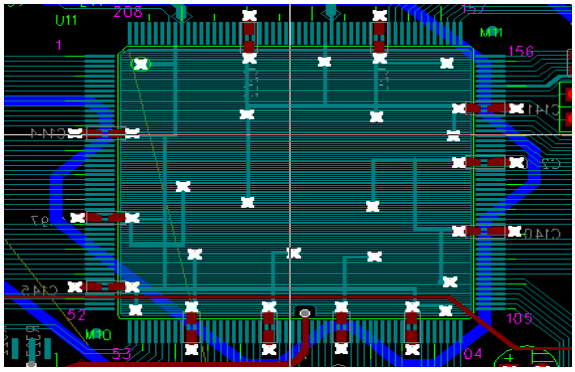
5.1 General Layout Guideline

Pay attention to layout throughout entire layout process is necessary .The following guide will help the customer achieve the maximum system performance.

.

- Use decoupling capacitors to decouple high frequency noise between chip's power and ground, must be as close as possible to IP108 LF. (Figure1)

Figure 1



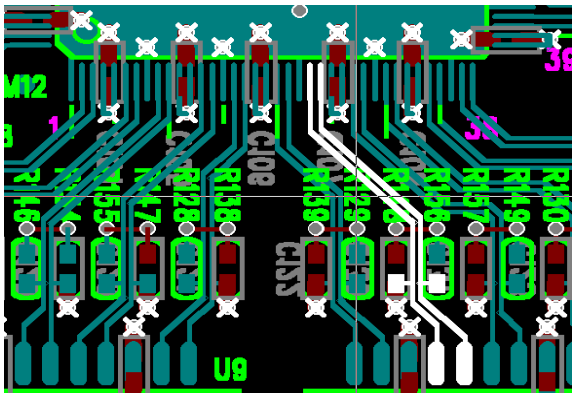
- Use guard traces around the clock trace to reduce the EMI effect.
- Avoid signals path parallel to clock signals path, such as MDC and X1signals. The clock signals will interfere with other parallel signals, degrading signal quality.
- Keep the clock jitter as low as possible. The clcok error should be less than 100ppm for 25/50/125Mhz
- Avoid high speed signal getting across ground gap to prevent large EMI effect
- Keep ground region as one continuous and unbroken plane
- Place a gap between the system ground and the chassis grounds
- No any ground loop exists on the chassis ground .
- Leave outer edge of PCB voided on all layer to minimize fringe effects.

5.2 Twisted Pair layout guideline

When routing the TD+/- signal traces from the IP108 LF to transformer, you should keep the trace as short as possible. The termination resistors should be as close as possible to the output of the TD+/- pair of IP108 LF,The central tap of primary winding of these transformers must be connected to analog 1.8V. It is recommended that RD+/- trace pair be routed far away from the other pairs, separating individual trace from one another.
In order to prevent the PCB from the ESD damage, iIt is recommended that the traces between the phone jack and the transformer are away from other signals at leaset 80 mils, including power ground

and chassis ground. The trace between the transformer and the RJ-45 phone jack should not pass any via, minimizing the impedence matching problem.

Figure 2



5.3 RMII layout guideline

In RMII mode, the clock is driven by external 50Mhz clock and the data toggles at the clock edge. In order to meet timing requirement, it is recommended that reasonable series resistors are used at RMII high speed signal such as REFCLK, TX data and RX data, reducing RMII signal reflection.

5.4 SS-SMI layout guideline

The IP108 LF provide slew rate function to adjust rise and fall times, balancing the high frequency energy and the I/O driving capability. For long distance high frequency trace, the adjustment of driving capability may be crucial to the EMI and the system stability.
In addition, the following rules can help the designer to achieve the required performance.

- Layout the traces as short as possible to minimize the high frequency energy radiation.
- Each signal tarce should be matched by a series resistor to maintain the signal quality.
- Keep the TXD[0],TXSYNC,TX_CLK signal traces matched in length as possible. Similarly the receive part behaves in the same way.

5.5 Power filter recommendation

In most application system, the power quality is very important, because the device maybe very sensitive to power noise, the Bead and the capacitor are often used. The Bead can prevent the high frequency from entering the power source. The capacitor can decouple noise by passing the noise to ground. These devices can reduce the noise ineterference and enhance system performance.
The decoupling capacitor (around 0.1uf to 0.01uf) should be placed at each pair of power pins to minimize the high frequency present at the power pins. The larger value capacitors, such as 10uf, should be scattered around the chip to stabilize the power input.

5.6 MDC and MDIO recommendation

In some high port count switch system, the driving source of MDC probably be routed for a long distance. For this application, the MDC can be buffered by a low slew rate driver and the trace at each driver output is terminated by a series resistor. The MDC should be kept away from other high speed signal, avoiding the interference to each other.

6 Electrical Characteristics

6.1 Absolute Maximum Rating

Permanent device damage may occur if Absolute Maximum Ratings are exceeded. Functional operation should be restricted to the conditions as specified in the Recommended Operating Conditions section. Exposure to the Absolute Maximum Conditions for extended periods may affect device reliability.

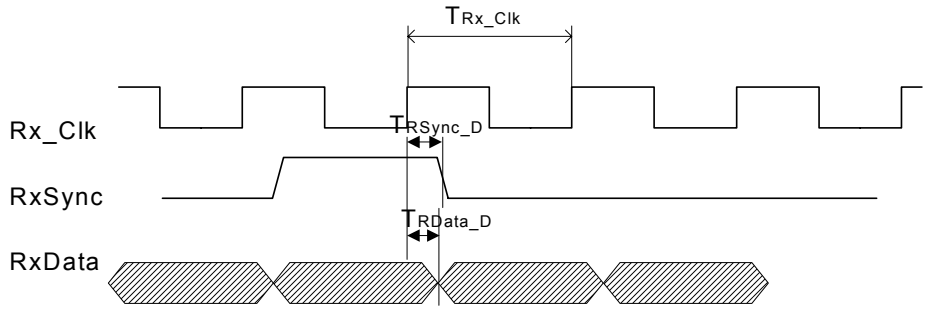
PARAMETER		SYMBOL	MIN.	MAX.	UNIT
Supply Voltage	I/O	$V_{DDI/O}$	– 0.5	+3.6V	V
	Core	V_{DDCore}	– 0.5	+1.9V	V
Input Voltage		V_I	– 0.5	$V_{DDI/O}$	V
Output Voltage		V_O	– 0.5	$V_{DDI/O}$	V
Storage Temperature		T_{STG}	-65	+150	°C
Operation Temperature		T_{OPT}	0	+70	°C

Note: The maximum ratings are the limit value that must never be exceeded even for short time.

6.2 AC Characteristics

SS-SMII Receive Timing

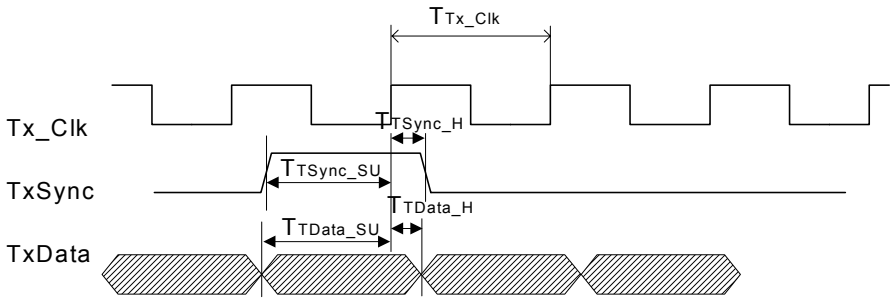
Symbol	Description	Min.	Typ.	Max.	Unit
T_{Rx_Clk}	Receive clock cycle time	-	8	-	ns
T_{RSync_D}	Rx_Clk to RX_Sync output delay	0.35		3.0	ns
T_{RData_D}	Rx_Clk to RXD output delay	0.35	-	3.0	ns



SS-SMII Receive

SS-SMII Transmit Timing

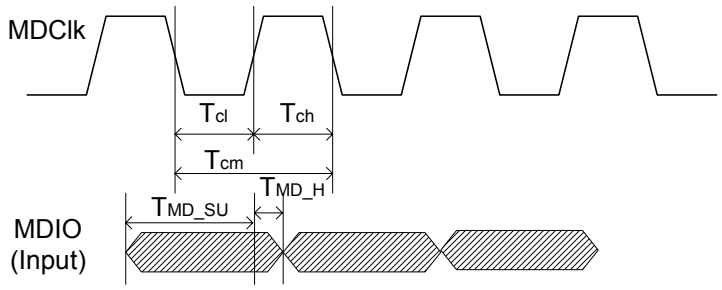
Symbol	Description	Min.	Typ.	Max.	Unit
T_{Rx_Clk}	Transmit clock cycle time	-	8	-	ns
T_{RSync_SU}	Tx_Sync Set up time	2.0			ns
T_{RData_H}	Tx_Sync Hold time	1.0	-		ns
T_{RData_SU}	TxData Set up time	2.0			ns
T_{RData_H}	TxData Hold time	1.0	-		ns



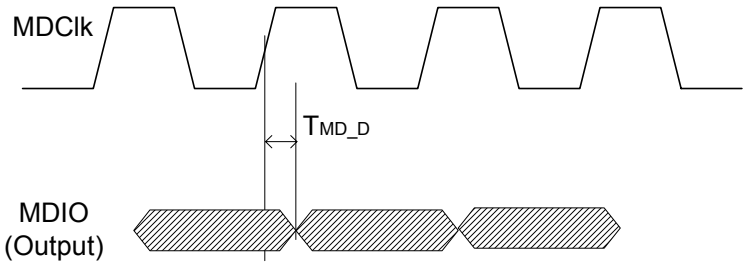
SS-SMII Transmit

PHY Management (MDIO) Timing

Symbol	Description	Min.	Typ.	Max.	Unit
T_{ch}	MDCK High Time				ns
T_{MD_SU}	MDIO set up time	10	-		ns
T_{MD_H}	MDIO hold time	10	-	-	ns
T_{MD_D}	MDIO output delay time	200	-	210	ns



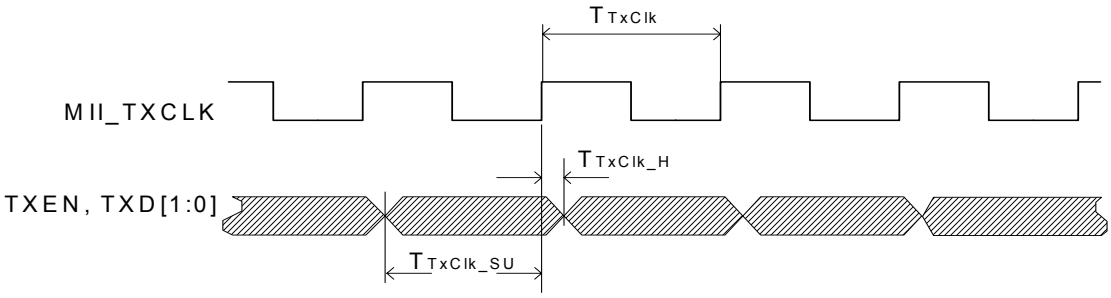
MDIO Input Cycle



MDIO Output Cicle

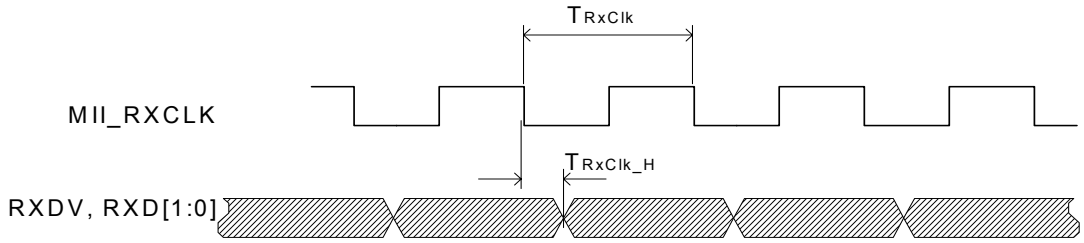
MII Transmit Timing

Symbol	Description	Min.	Typ.	Max.	Unit
T_{TxClk}	Transmit clock period	-	20	-	Ns
T_{TxClk_SU}	MII_TXCLK to TXEN, TXD setup time	2	-	-	Ns
T_{TxClk_H}	MII_TXCLK to TXEN, TXD hold time	1	-	-	Ns



MII Receive Timing

Symbol	Description	Min.	Typ.	Max.	Unit
T_{RxClk}	Receive clock period	-	20	-	Ns
T_{RxClk_D}	MII_RXCLK falling edge to RXDV, RXD Delay	1	-	4	Ns



6.3 DC Characteristics

PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT
Output low voltage	V_{OL}			0.4	V
Output high voltage	V_{OH}	1.7V for 1.8V I/O supply voltage; 3V for 3.3V I/O supply voltage;			V
Low level output current	I_{OL}				mA
High level output current	I_{OH}				
VDD33 supply current					
VDD18 supply current					
VDDPLL supply current					
Input Treshold point	V_T	1.46	1.60	1.76	V
SS-SMII Input Low to High treshold point *1	V_{T+}	1.66	1.75	1.79	V

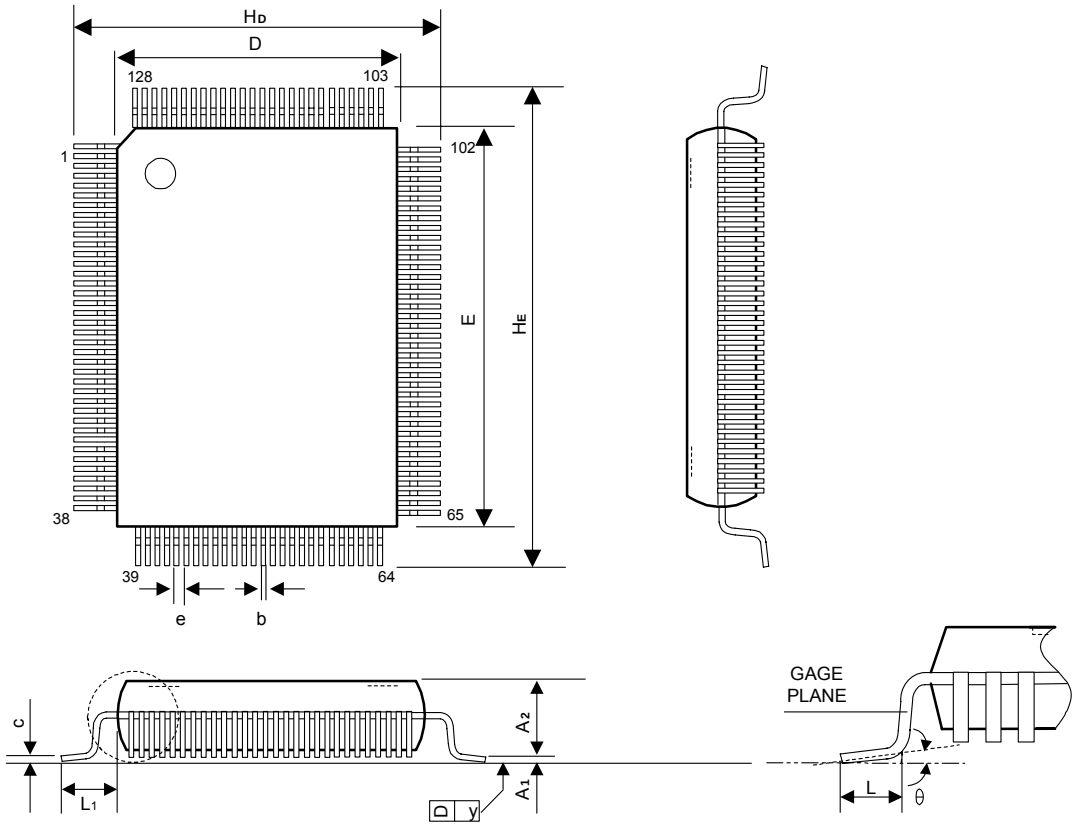
SS-SMII Input High to Low treshold point *1	V_{T-}	0.93	1.01	1.06	V
Pull-down resistor	R_{PD}	51		127	KΩ

7 Order Information

Part No.	Package	Notice
IP108	128 PIN QFP	-
IP108 LF	128 PIN QFP	Lead free

8 Package Detail

PQFP 128 (14mm x 20mm) Outline Dimensions Unit: inches/mm



Symbol	Dimensions In Inches			Dimensions In mm		
	Min.	Nom.	Max.	Min.	Nom.	Max.
A1	0.010	0.014	0.018	0.25	0.35	0.45
A2	0.107	0.112	0.117	2.73	2.85	2.97
b	0.007	0.009	0.011	0.17	0.22	0.27
c	0.004	0.006	0.008	0.09	0.15	0.20
HD	0.669	0.677	0.685	17.00	17.20	17.40
D	0.547	0.551	0.555	13.90	14.00	14.10
HE	0.906	0.913	0.921	23.00	23.20	23.40
E	0.783	0.787	0.791	19.90	20.00	20.10
e	-	0.020	-	-	0.50	-
L	0.025	0.035	0.041	0.65	0.88	1.03
L1	-	0.063	-	-	1.60	-
y	-	-	0.004	-	-	0.10
θ	0°	-	12°	0°	-	12°

Note:
1. Dimension D & E do not include mold protrusion.
2. Dimension B does not include dambar protrusion. Total in excess of the B dimension at maximum material condition. Dambar cannot be located on the lower radius of the foot.